

# AKN62314B Series

# AKN62334B Series

524288-Word × 8-Bit CMOS Mask Programmable ROM

AKN62314B, AKN62334B Series is a 4-Mbit CMOS mask-programmable ROM organized as 524288-word x 8-bits. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

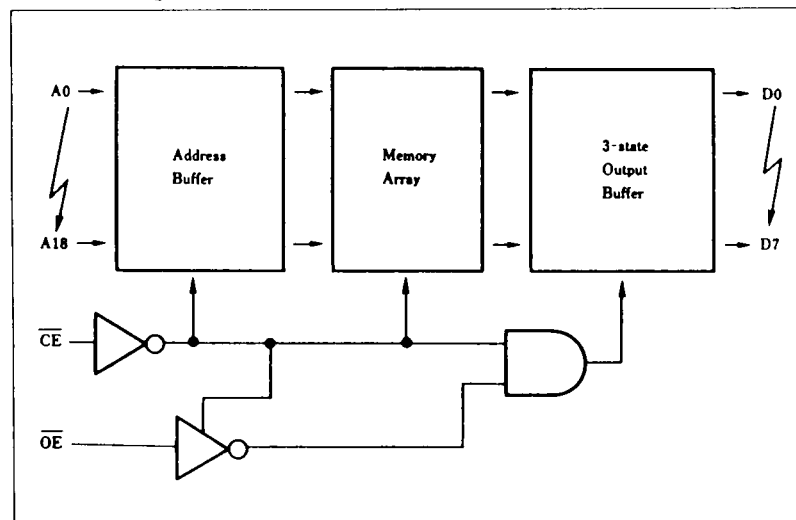
## Features

- Single +5V power supply
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/170/200 ns (max.)
- Low power: Active 100 mW (typ)  
Standby 5  $\mu$ W (typ)
- Byte-Wide Data Organization
- Pin-compatible with JEDEC

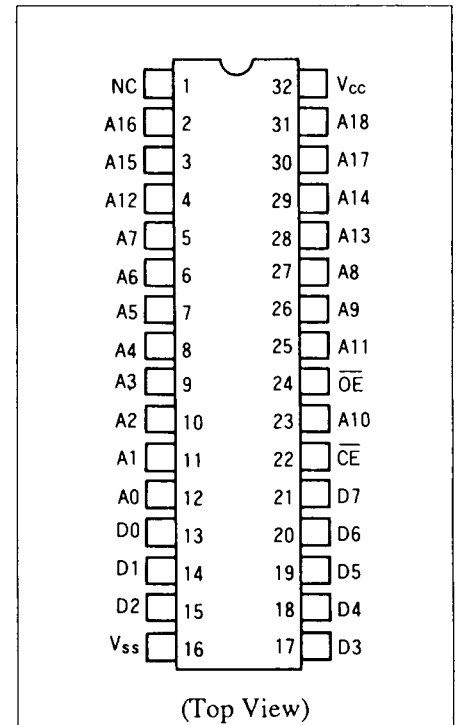
## Ordering Information

Type No.	Address Access Time	Package
AKN62314BP-20	200 ns	600 mil 32-pin plastic DIP
AKN62314BP-17	170 ns	
AKN62334BP	150 ns	
AKN62314BF-20	200 ns	32-pin plastic SOP
AKN62314BF-17	170 ns	
AKN62334BF	150 ns	

## Block Diagram



## PIN CONFIGURATION



## Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V <sub>CC</sub>	-0.3 to +7.0	V
Terminal voltage*1	V <sub>T</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C
Bias temperature	T <sub>bias</sub>	-20 to +85	°C

Note: \*1. With respect to V<sub>SS</sub>.

## Recommended Operating Conditions (V<sub>SS</sub> = 0 V, T<sub>a</sub> = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>	-0.3	—	0.8	V

## DC Characteristics (V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V, T<sub>a</sub> = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I <sub>CC</sub>	—	50	mA	V <sub>CC</sub> = 5.5 V, I <sub>DOUT</sub> = 0 mA, t <sub>RC</sub> = Min
	Standby	I <sub>SB</sub>	—	30	μA	V <sub>CC</sub> = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		I <sub>LI</sub>	—	10	μA	V <sub>IN</sub> = 0 to V <sub>CC</sub>
Output leak current		I <sub>LO</sub>	—	10	μA	$\overline{CE} = 2.2$ V, V <sub>OUT</sub> = 0 to V <sub>CC</sub>
Output voltage		V <sub>OH</sub>	2.4	—	V	I <sub>OH</sub> = -205 μA
		V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 1.6 mA

## Capacitance (V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V, T<sub>a</sub> = 25°C, V<sub>in</sub> = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	C <sub>in</sub>	—	15	pF
Output capacitance*1	C <sub>out</sub>	—	15	pF

Note: \*1. This parameter is sampled and not 100% tested.

## AC Operating Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $T_a = 0\text{ to }+70^\circ\text{C}$ )

### Test Conditions

Input pulse level: 0.8 to 2.4 V

I/O timing reference level: 1.5 V

Input rise/fall time: 10 ns

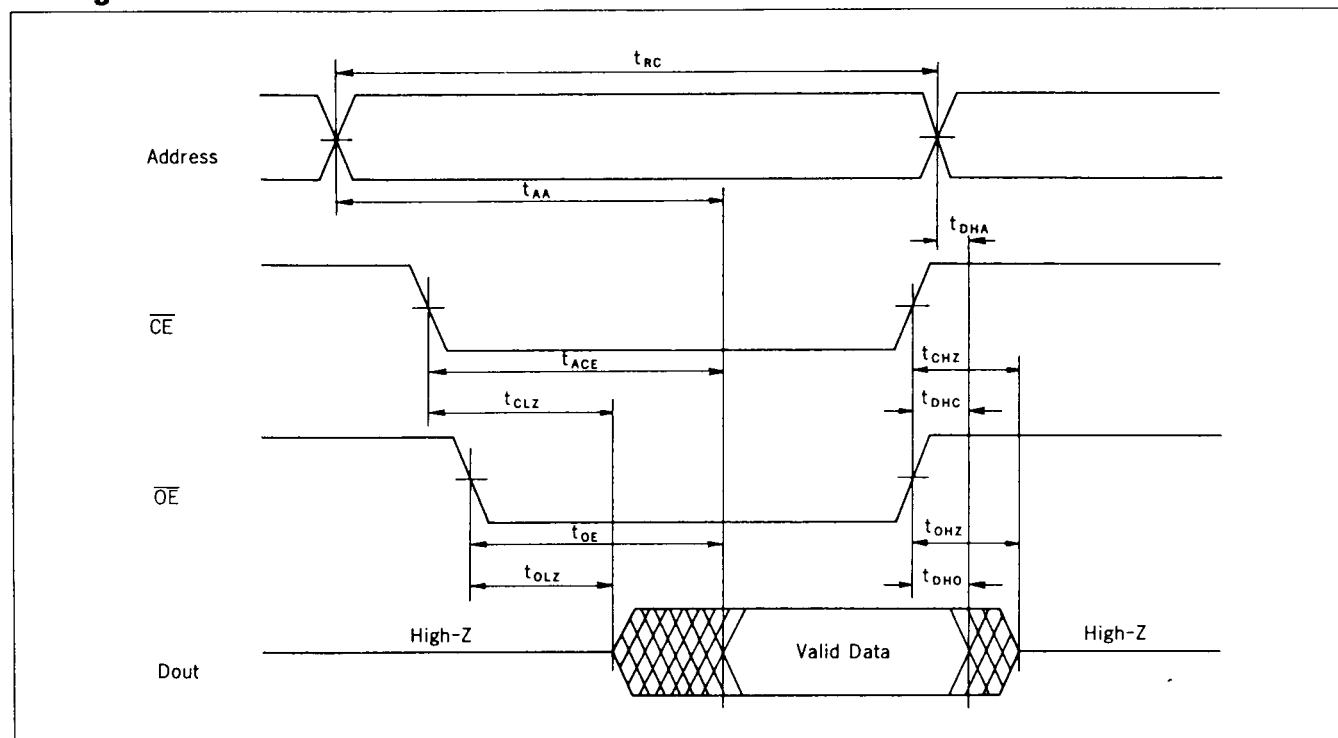
Output load:

1 TTL gate +  $C_L = 100\text{ pF}$   
(including jig capacitance)

Item	Symbol	AKN62334B		AKN62314B-17		AKN62314B-20		Unit
		Min	Max	Min	Max	Min	Max	
Cycle time	$t_{RC}$	150	—	170	—	200	—	ns
Address access time	$t_{AA}$	—	150	—	170	—	200	ns
$\overline{CE}$ access time	$t_{ACE}$	—	150	—	170	—	200	ns
$\overline{OE}$ access time	$t_{OE}$	—	70	—	70	—	100	ns
Output Hold Time from Address Change	$t_{DHA}$	0	—	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	$t_{DHC}$	0	—	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	$t_{DHO}$	0	—	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	$t_{CHZ}^{*1}$	—	70	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	$t_{OHZ}^{*1}$	—	70	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	$t_{CLZ}$	10	—	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	$t_{OLZ}$	10	—	10	—	10	—	ns

Note: \*1  $t_{CHZ}$  and  $t_{OHZ}$  define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

### Timing Waveform



- Notes:
1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$ ; Determined by whichever is faster.
  2.  $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$ ; Determined by whichever is slower.
  3.  $t_{CLZ}$ ,  $t_{OLZ}$ ; Determined by whichever is slower.